

## REMARKS

Applicant will address each of the Examiner's objections and rejections in the order in which they appear in the Office Action.

### Claim Objection

In the Office Action, the Examiner objects to Claims 54-59 for an informality and in particular, for lacking an antecedent basis for "the semiconductor layer." The Examiner suggests that the term be changed to "the semiconductor film."

As Applicants have amended these claims in accordance with the Examiner's suggestion, it is respectfully submitted that the Examiner's objection has been overcome, and it is requested that the objection be withdrawn.

### Claim Rejections - 35 USC §103

#### Claims 24, 25, 28, 39, 41, 43, 54 and 57

The Examiner also rejects Claims 24, 25, 28, 39, 41, 43, 54 and 57 under 35 USC §103(a) as being unpatentable over Zaleski (US 5,455,791) together with Yamazaki et al. (US 6,127,702). This rejection is respectfully traversed.

More specifically, independent Claims 24 and 39 recite that "the floating gate overlaps a boundary between at least one of the pair of the first impurity regions and the at least two second impurity regions."

The Examiner admits that Zaleski does not disclose this claimed feature. The Examiner, however, cites Yamazaki and contends that it discloses a thin film transistor with at least two such impurity regions (104 in Fig. 1 in Yamazaki) which connect source and drain regions 101 and 102. The Examiner then concludes that "[i]t would have been obvious to one skilled in the

art to provide Zaleski's thin film transistor with at least two such second impurity regions that connect source and drain regions 4b and 4a (resulting in a semiconductor device whose floating gate overlaps a boundary between at least one of the source and drain regions (i.e. at least one of the pair of first impurity regions) and the at least two second impurity regions) in order to suppress short channel effects as taught by Yamazaki." [Emphasis in original]. Applicant respectfully disagrees.

Yamazaki appears to disclose as a boundary between impurity region (pinning region) 104 and the source 101 or drain 102, and a boundary between channel region 103 and the source 101 or drain 102. Zaleski appears to disclose a floating gate 6 that overlaps the boundary between the channel region 4c and source 4b or drain 4a.

However, as shown in Fig. 1A of Yamazaki, the boundary between the impurity region (pinning region) 104 and the source 101 or drain 102 appears to be located apart from the boundary between the channel region 103 and the source 101 or drain 103. Hence, even if these two references were combinable (which Applicant does not admit), the combination would still not include the feature of "wherein the floating gate overlaps a boundary between at least one of the pair of the first impurity regions and the at least two second impurity regions" of independent Claims 24 and 39 of the present application.

Accordingly, Claims 24 and 39 and those claims dependent thereon are patentable over the cited references, and it is respectfully requested that this rejection be withdrawn.

Claims 29, 30, 33, 34, 35, 38, 44, 46, 48, 49, 51, 53, 55, 56, 58 and 59

The Examiner also rejects Claims 29, 30, 33, 34, 35, 38, 44, 46, 48, 49, 51, 53, 55, 56, 58 and 59 under 35 USC §103(a) as being unpatentable over Zaleski et al. together with Yamazaki et al. and Liu (US 5,814,854). This rejection is also respectfully traversed.

For similar reasons to those discussed above, independent Claims 29, 34, 44 and 49 and those claims dependent thereon are also not disclosed or suggested by the cited references but are patentable thereover.

Accordingly, it is respectfully requested that this rejection be withdrawn.


### Conclusion

Accordingly, it is respectfully submitted that the present application is in a condition for allowance and should be allowed.

If any further fee is due for this amendment, please charge our deposit account 50/1039.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,

  
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